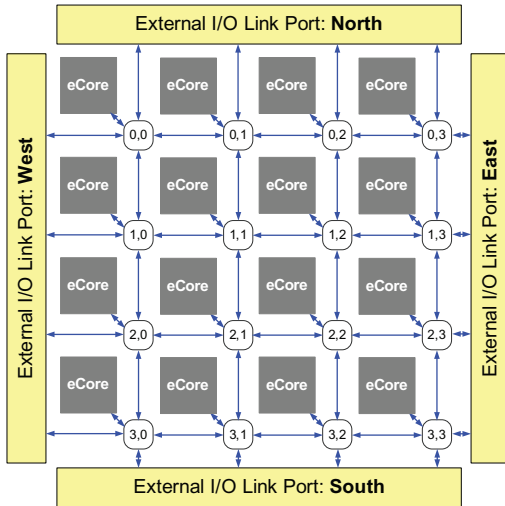


Anemone™ Co-Processor for FPGAs

Low-Power, C-Programmable, Floating Point



- 16 independent floating point cores
- 32 GFLOPS of floating point processing
- 2 Watts total chip power
- ANSI C-programmable
- IEEE Floating Point
- Shared memory architecture
- External I/O via memory-mapped links
- Scale multiple chips up to 8 TFLOPS
- High throughput mesh network
- Standard GNU/Eclipse Development Tools
- Available from BittWare on standard board formats

A New Approach to Floating Point DSP

Traditional floating point DSPs, while excellent at complex processing tasks, have limitations when it comes to chip real estate and power efficiency that have caused them to become an endangered species. And FPGAs, while superior for versatility and configurability, can be difficult to use for complex and evolving applications. The BittWare Anemone, featuring the Epiphany architecture from Adapteva, enables the best assets of both to be combined, thereby offering a completely new approach to floating point digital signal processing. This hybrid solution provides a standard processor software development environment working in conjunction with a world-class FPGA platform, allowing users to optimally partition their algorithms into hardware and software. The result is superior development productivity and unmatched system size, weight, and power.

Focus on power & efficiency

Anemone is a truly C-programmable floating point compute engine. It is unique in that it achieves superior power efficiency and processing performance because it is designed to work alongside an FPGA as a co-processor. The FPGA handles all the memory, I/O interfacing, protocol processing, and special functions in addition to any computational tasks it may perform, leaving the Anemone free to efficiently perform the complex processing tasks that DSPs are ideal for. This allows Anemone to be an extremely efficient chip - as compared with traditional floating point DSPs that may only use 5% of the silicon area for processing.

Simple, elegantly designed floating point cores

The Anemone is a completely scalable, up to 1 GHz multicore processor with 16 eCores that provide a total sustained performance of 32 GFLOPS while consuming only 2 Watts of total chip power. Each eCore features a compact, general-purpose instruction set that requires no instruction level parallelism and provides high program efficiency. All floating point computations are performed as single-precision IEEE 754; hardware looping is also supported. Anemone offers distributed and segmented memory, and



large uniform register files. On-chip distributed shared memory is 4 Mb (32 KByte per eCore) with 32 GBytes/sec of sustained memory bandwidth within each eCore. The cache-less shared memory architecture is extended off-chip via I/O links.

High-throughput eMesh network

The Anemone features an internal high-throughput mesh network, with separate data paths for on-chip and off-chip communications. Each eCore has a multi-channel DMA engine to support background data movement over the mesh. Total on-chip, inter-core bandwidth is 128 GBytes/sec full duplex, with an additional 8 GBytes/sec of off-chip bandwidth. Each router node can simultaneously sustain full-duplex transfers on all ports, with automatic routing based on global addressing.

I/O via memory-mapped high-speed links

The Anemone provides a flexible low-overhead external interconnect scheme that supports memory-mapped direct connection of multiple Anemones and is compatible with any LVDS capable FPGA. This is achieved via four links that are full-duplex 8-bit LVDS data ports @ 500 MHz DDR, each simultaneously providing 1 GByte/sec in each direction for a total off-chip bandwidth of 8 GBytes/sec. Its FPGA co-processor use model provides the ultimate flexibility: since all external I/O goes through an FPGA, system designers can customize the I/O to their application's specific requirements.

ANSI C-programmable; Standard GNU development tools

The Anemone reduces system development cost by enabling out-of-the-box execution of applications written in regular ANSI-C. It does not require any C-subset, language extensions, or SIMD. Standard GNU development tools are supported including an optimizing C compiler, simulator, GDB debugger, and Eclipse multi-core IDE.

Available on standard board form factors

The Anemone is available from BittWare on standard board form factors, including FMC (VITA 57), AdvancedMC (AMC), VPX (VITA 46/48/65), and PCI Express (PCIe) slot card. Development boards and systems are also available.

Anemone: A New Approach to Floating Point DSP

Specifications

PERFORMANCE/POWER

- 32 GFLOPS
- 2 Watts total chip power

EPIPHANY eCORE

Anemone has 16 independent eCores, each with:

FPU: Floating-Point Unit

- 2 FLOP (1 MAC) per cycle
- 2 GFLOPS @ 1GHz
- Single precision IEEE 754 floating point
- Shared memory multiprocessor architecture
- C-friendly instruction set
- Hardware looping

Register File

- Flat, uniform file of 64 entries
- Single load/store model

Network Interface & DMA

- Shared memory-mapped, transparent to eCore
- Full duplex 8 GBytes/sec bandwidth per eCore
- 2 DMA channels per eCore @ 1 GHz each
- Supports background I/O

IALU: Integer Arithmetic Unit

- Address generation

Segmented Memory

- 32 KBytes SRAM per eCore (512 KB total; 4 banks of 8 KByte)
- 32 GBytes/sec memory bandwidth
- Cache-less
- Shared memory architecture

EPIPHANY eMESH NETWORK

3 independent, full-duplex mesh networks:

Networks

- cMesh for core writes (on-chip): 8 GBytes/sec each direction, per segment
- xMesh for external writes (off-chip): 1 GByte/sec each direction, per segment
- rMesh for read requests: 1 GByte/sec each direction, per segment

Transparently Shared Memory

- Routing operates independently of cores
- Coordinate based routing
- Extends off-chip, supporting up to 4096 eCores in a single 2D mesh

Clock

- 1 GHz full clock rate

I/O AND DEBUG PORTS

External I/O Link Ports

- 8 GBytes/sec off-chip bandwidth
- 4 memory-mapped link ports
- Full-duplex 8-bit LVDS @ 500 MHz DDR

SPI Port

- Allows debug, command, & control
- Access to every core, register, & memory

DEVELOPMENT TOOLS

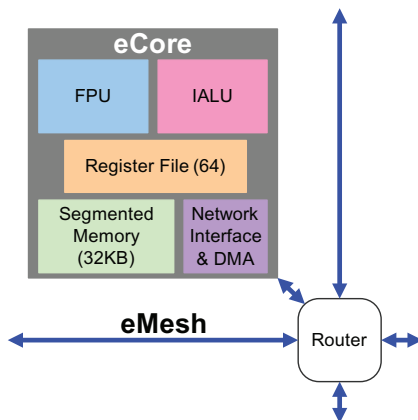
Adapteva Epiphany SDK

- Optimized GNU C compiler w/ binutils
- Simulator
- Standard GNU GDB debugger
- Eclipse multi-core IDE

AVAILABLE BOARD FORM FACTORS

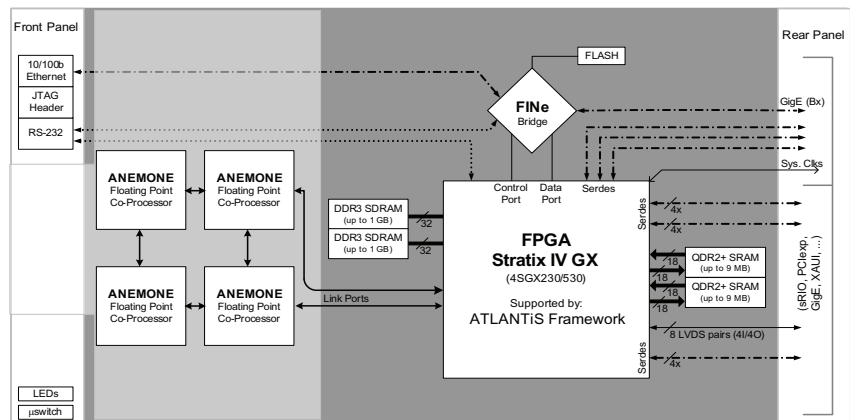
- FMC (VITA 57) FPGA Mezzanine Card
- VPX (VITA 46/48/65)
- AMC (AdvancedMC) for MicroTCA & ATCA
- PCI Express (PCIe) slot card

Figure 1: eCore Block Diagram



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Figure 2: Anemone FMC on a BitWare FPGA Carrier Board



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