A5-PCIe-L

Altera Arria® V GZ Low Profile PCIe Board with Dual QSFP+ and DDR3, QDRII+, or RLDRAM3

- High performance Altera Arria V GZ FPGA
- PCIe x8 interface supporting Gen1, Gen2, or Gen3
- Dual QSFP+ cages for 2x 40GigE or 8x 10GigE
- Memory options:
  - up to 8 GBytes of DDR3 SDRAM with ECC
  - up to 512 MBytes RLDRAM3
  - up to 72 MBytes QDRII+
- Board Management Controller for Intelligent Platform Management
- USB 2.0 for programming and debug
- Timestamping and synchronization support

BittWare's A5-PCIe-L (A5PL) is a low-profile PCIe x8 card based on the Altera Arria V GZ FPGA. The high-performance, power- and cost-efficient Arria V GZ provides a high level of system integration and flexibility for I/O, routing, and processing. Up to 8 GBytes of on-board memory includes DDR3, QDRII/II+, or RLDRAM3. Two front-panel QSFP+ cages allow two 40GigE or eight 10GigE interfaces direct to the FPGA. The A5PL also features a Board Management Controller (BMC) for advanced system monitoring, which greatly simplifies platform management. All of these features combine to make the A5PL a versatile and efficient solution for network processing, security, broadcast, and signals intelligence applications.

Altera Arria V GZ FPGA

The 28nm Arria V family of FPGAs deliver optimal performance, power, and cost efficiency for mid-range applications. The Arria V GZ variant, which is featured on the S5PL, offers the highest bandwidth of the Arria V FPGAs. The Arria V GZ provides Gen3 PCIe x8 via a hard IP block and features 16 full-duplex transceivers with data rates up to 12.5 Gbps, and up to 450K equivalent LEs.

I/O Interfaces

The A5PL provides a variety of interfaces for high-speed serial I/O as well as debug support. Two QSFP+ cages are available on the front panel, each supporting 40GigE or four 10GigE channels using optical transceivers as well as passive copper cabling up to 8 meters. The QSFP+ SerDes channels are connected directly to the Arria V GZ FPGA, thus removing the latency of external PHYs. The QSFP+ cages can optionally be adapted for SFP+.

The Gen3 x8 PCIe interface provides 8 SerDes lanes to the Arria V GZ FPGA. An optional USB 2.0 interface is available for debug and programming support.

Timestamping and Synchronization

The board supports timestamping and synchronization with optional SMA connectors on the front panel for a 1 PPS and reference clock input.* A tunable, high accuracy, temperature compensated oscillator (TCXO) and a programmable clock synthesizer (Si5338) provide sophisticated timing and clocking options. IP is also available for IEEE 1588 Precision Time Protocol (PTP).

Memory

The A5PL features an extremely flexible memory configuration, with a SODIMM site that supports DDR3 SDRAM, RLDRAM3, and QDRII+. Memory card options include the following: up to 8 GBytes of DDR3 with optional error-correcting codes (ECC); up to 36 MBytes QDRII+ (2 banks x18); or up to 512 MBytes RLDRAM3 (2 banks x18). Additional on-board memory includes flash memory for storing multiple FPGA images. An on-board PROM provides access to the board's MAC ID.

* *Requires full-height front panel*

Board Management Controller

Boards in BittWare's A5 family feature an advanced system monitoring subsystem, similar to those typically found on today's server platforms. At the heart of the board's monitoring system lies a Board Management Controller (BMC), which accepts Intelligent Platform Management Interface (IPMI) messaging protocol commands. The BMC provides a wealth of features, including control of power and resets, monitoring of board sensors, FPGA boot loader, voltage overrides, configuration of programmable clocks, access to I^2C bus components, field upgrades, and IPMI messaging. Access to the BMC is via PCIe or USB. BittWare's BittWorks II Toolkit also provides utilities and libraries for communicating with the BMC components at a higher, more abstract level, allowing developers to remotely monitor the health of the board.

Development Tools

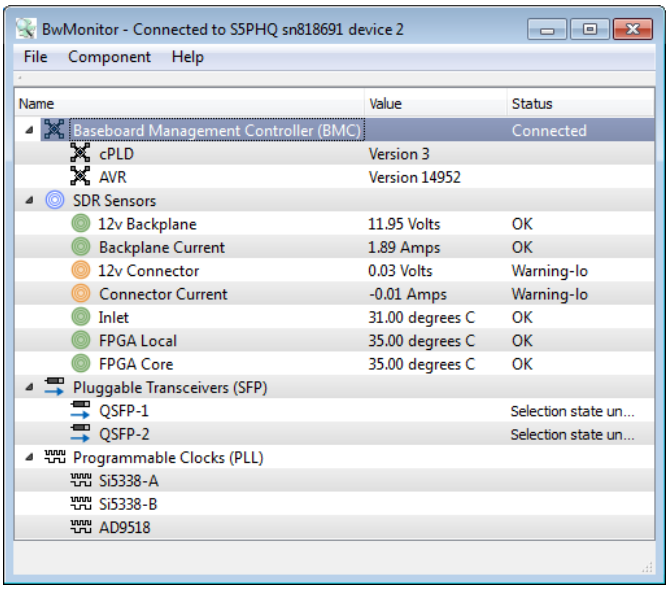
BittWorks II Toolkit

BittWare offers complete software support for the A5PL with its BittWorks II software tools. Designed to make developing and debugging applications for BittWare's boards easy and efficient, the Toolkit is a collection of libraries and applications that provides the glue between the host application and the hardware. A variety of features allow developers to take full advantage of the Arria V GZ FPGA capabilities on the BittWare board, including FPGA control via PCIe, Flash programming, custom ISR scripts, and convenient control of FPGA loads. The Toolkit supports 32-bit, and 64-bit Windows and Linux platforms and can connect to the board via PCIe or USB, providing a common API no matter the connection method.

FPGA Development Kit

BittWare's FPGA Development Kit (FDK) provides FPGA board support IP and integration for BittWare's Altera FPGA-based boards. The FDK includes FPGA components that provide preconfigured physical interfaces, infrastructure, and examples, drastically cutting development time and easily integrating into existing FPGA development environments.

Working example projects are available for each board which illustrate how to move data between the board's different interfaces. Supported interfaces include DDR3, DDR2, QDR2/+, PCIe, 10GigE, LVDS, SerDes, and Double Data Rate I/O. All example projects are available on BittWare's Developer Site.



BwMonitor in the BittWorks II Toolkit provides a view into the baseboard management capabilities of your BittWare hardware.

BittWare Firmware and Network Solutions Partners

BittWare offers firmware for the Arria V GZ FPGA on the A5 family PCIe boards, targeted specifically for networking applications. BittWare's FPGA framework provides a solid base for your application, including the following:

- 10GigE MAC
- PCIe multi-channel DMA engines
- DDR3 SDRAM and QDRII/II+ controllers

BittWare has also partnered with several companies to offer solutions for networking and financial acceleration:

- LeWiz: Ultra low latency, multi-session TOE IP cores
- Intilop: Ultra low latency TOE, UOE, and MAC
- PolyBus: Infiniband link layer and transport layer
- Algo-Logic: Market feed handler and low latency gateway libraries
- Fraunhofer HHI: 10GigE TCP & UDP offload engines, 10GigE MACS and custom services
- Enyx: UOE, TOE, book building IP, order management IP, Market Feed Handler
- InDeLabs: Market Data Feed Handler and custom services
- Network Allies: IBM and Intel server computing systems
- PLDA: Low latency TCP/IP offload engine, UDP and PCIe IP cores
- Tamba Networks: Lowest latency 10/40 GigE MAC + PCS

A5-PCIe-L Specifications

Board Specifications

FPGA

- Altera® Arria® V GZ FPGA
- Up to 16 full-duplex, high-performance, multi-gigabit SerDes transceivers @ up to 12.5 GHz
- Up to 450K logic elements available
- Up to 34 Mb of embedded memory
- 1.6 Gbps LVDS performance
- Up to 2278 18x18 multipliers

On-Board Memory

- Flash memory for booting FPGA

Optional SODIMM

- DDR3: x72 w/ECC
  - Up to 8 GB per SODIMM
- RLDRAM3: 2x banks of x18
  - 2x (32 M x 18): 128 MB per SODIMM
  - 2x (64 M x 18): 256 MB per SODIMM
  - 2x (128M x 18): 512 MB per SODIMM
- QDRII+: 2x banks of x18
  - 2x (4 MB x 18): 18 MB per SODIMM
  - 2x (8 MB x 18): 36 MB per SODIMM

PCIe Interface

- x8 Gen1, Gen2, Gen3 direct to FPGA

USB Header

- USB 2.0 interface for debug and programming FPGA and Flash

Timestamp and Synchronization (Optional)

- 2 front panel SMA connectors*
  - 1 PPS input
  - Reference clock input
- Tunable high-accuracy TCXO
- Programmable clock synthesizer (Si5338)

QSFP+ Cages

- 2 QSFP+ cages on front panel connected directly to FPGA via 8 SerDes (no external PHY)
- Each supports 40GigE or 4 10GigE
- Can be optionally adapted for use as SFP+

Baseboard Management Controller

- Voltage, current, temperature monitoring
- Power sequencing and reset
- Field upgrades
- FPGA configuration and control
- Clock configuration
- I²C bus access
- USB 2.0 access
- Voltage overrides

Size

- Half-height, half-length (low profile) PCIe slot card

Development Tools

System Development

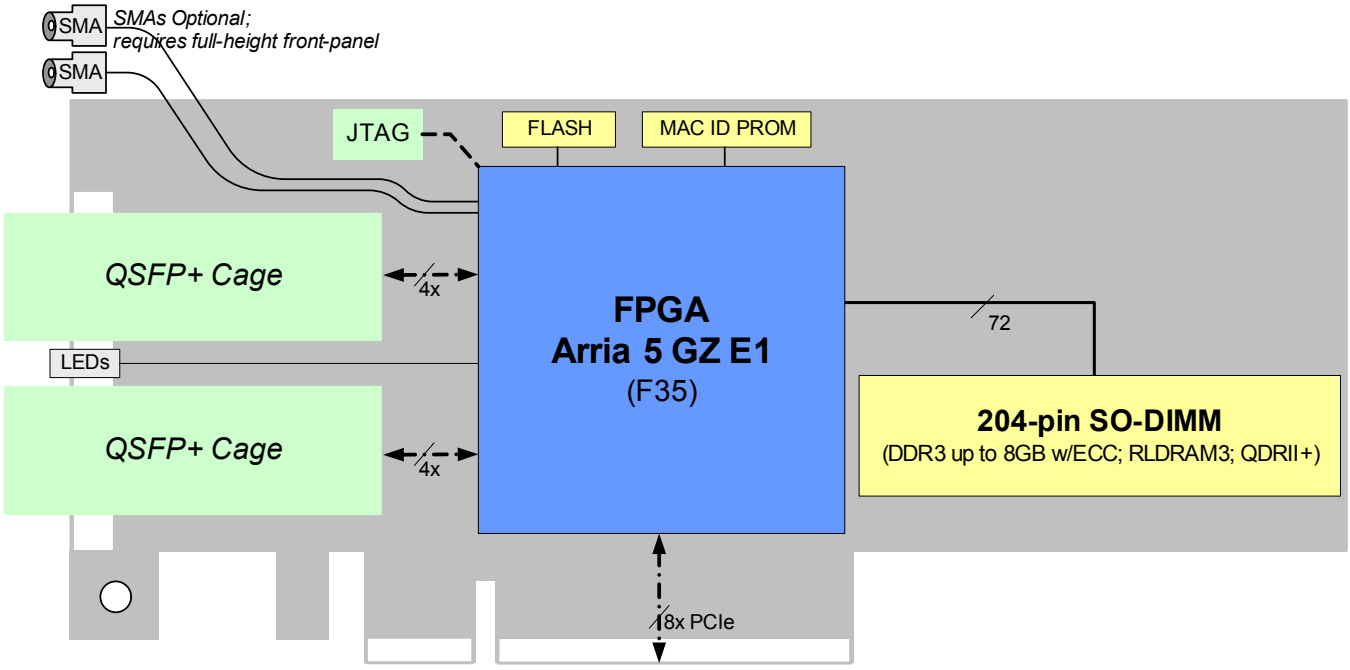
- BittWorks II Toolkit - host, command, and debug tools for BittWare hardware; source code porting kit also available

FPGA Development

- FPGA Development Kit
  - Physical interface components
  - Board, I/O, and timing constraints
  - Example Quartus projects
  - Software components and drivers
- Altera Tools
  - Quartus II software

* *Requires full-height front panel*

Figure 2: A5PL System Block Diagram



A5PL Ordering Options

A5PL-RW-AAAAAAAA-BB-CDE-F

RW	**Ruggedization** 0U = Commercial (0C to 50C)*	C	**Oscillator** N = None T = TCXO A = Adjustable TCXO
AAAAAAAA	**Arria V Family, HardIP, and Size** GZME12C3 - Arria V GZME12C3* GZME32C3 - Arria V GZME32C3 GZME52C3 - Arria V GZME52C3 GZME72C3 - Arria V GZME72C3	D	**Timing** 0 = Not installed X = External Sync
BB	**SODIMM** 00 = None 99 = No socket D3 = DDR3 8GB x72* QB = QDRII+ 72MB 2x18 R3 = RLDRAM3 512MB 2x18 †	E	**Misc. Configuration** 0 = Standard
		F	**Envelope Assembly** 6 = RoHS 6/6*

* Default
† Contact BittWare for availability

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BittWare FPGA COMPUTING SYSTEMS