S5-PCIe-HQ

Altera Stratix® V GX/GS Half-Length PCIe Board with Dual QSFP+/SFP+, DDR3, and QDRII+

- High density Altera Stratix V GX/GS FPGA
- PCIe x8 interface supporting Gen1, Gen2, or Gen3
- Dual QSFP+ cages for 40GigE or 10GigE direct to the FPGA for lowest possible latency
- Anemone floating point co-processor (optional)
- Up to 8 GBytes DDR3 SDRAM
- Up to 72 MBytes QDRII/II+
- Two SATA connectors
- Utility I/O includes: USB 2.0, RS-232, and JTAG

BittWare's S5-PCIe-HQ (S5PH-Q) is a half-length PCIe x8 card based on the high-bandwidth, power-efficient Altera Stratix V GX or GS FPGA. Designed for high-end applications, the Stratix V provides a high level of system integration and flexibility for I/O, routing, and processing. The S5PH-Q is a versatile and efficient solution for high-performance network processing, signal processing, and data acquisition. Combining it with BittWare's Anemone co-processor and ATLANTiS FrameWork enhances productivity and portability and allows even greater processing efficiency. Over 8 GBytes of on-board memory includes DDR3 and QDRII/II+. Providing additional flexibility are two front-panel QSFP+ cages for serial I/O, allowing two 40GigE interfaces (or eight 10GigE), direct to the FPGA for reduced latency, making it ideal for high frequency trading and networking applications.

Altera Stratix V GX/GS FPGA

The Altera Stratix V FPGA is optimized for high-performance, high-bandwidth applications with integrated transceivers supporting backplanes and optical modules. It supports 1.6 Tbps of serial switching capability and up to 3,926 18 x 18 variable precision multipliers. The Stratix V also provides PCI Express x8 via a hard IP block and supports configuration by PCI Express using the existing PCI Express link in your application. For additional flexibility, the Stratix V supports transceiver and core reconfiguration on-the-fly while other portions of the design are running. The FPGA is supported by BittWare's ATLANTiS FrameWork and provides seamless routing of all on-board data, I/O, and memory.

I/O Interfaces

The S5PH-Q provides a variety of interfaces for high-speed serial I/O as well as debug support. Two QSFP+ cages are available on the front panel, each supporting 40GigE or four 10GigE channels. The QSFP+ SerDes channels are connected directly to the Stratix V FPGA, thus removing the latency of external PHYs. The QSFP+ cages can optionally be adapted for SFP+.

Two SATA connectors are provided to connect external storage devices with the FPGA via two SerDes lanes. The x8 PCIe interface provides 8 SerDes lanes to the Stratix V FPGA. USB 2.0, RS-232, and JTAG interfaces are available for debug and programming support.

On-Board Memory

Several on-board memory banks are available to the Stratix V FPGA. Memory includes up to 8 GBytes of DDR3 (two 64-bit banks) and up to 72 MBytes QDRII/II+ (four 18-bit banks). The S5PH-Q also provides flash memory for FPGA images.

Value-Add Products for FPGA

BittWare's value-add products for FPGA ease development on our FPGA hardware and facilitate design portability and reuse, allowing our COTS boards to be ready to use off the shelf.

Anemone: Floating Point Co-processor for FPGA

An optional Anemone104 processor is available on the S5PH-Q as a co-processor for the Stratix V FPGA. Anemone is a truly C-programmable floating point compute engine that achieves superior power efficiency and processing performance by working alongside an FPGA as a co-processor. The FPGA handles all the memory, I/O interfacing, protocol processing, and special functions, in addition to any computational tasks it may perform. This leaves the Anemone free to efficiently perform complex processing tasks.

In addition to accelerating algorithmic performance, Anemone enables partitioning of processing between software and hardware, and it reduces system development cost by enabling out-of-the box execution of applications written in regular ANSI-C. Ideal for implementing complex algorithms and for implementing processing with changing requirements, Anemone is a low risk and low power way to add processing resources.

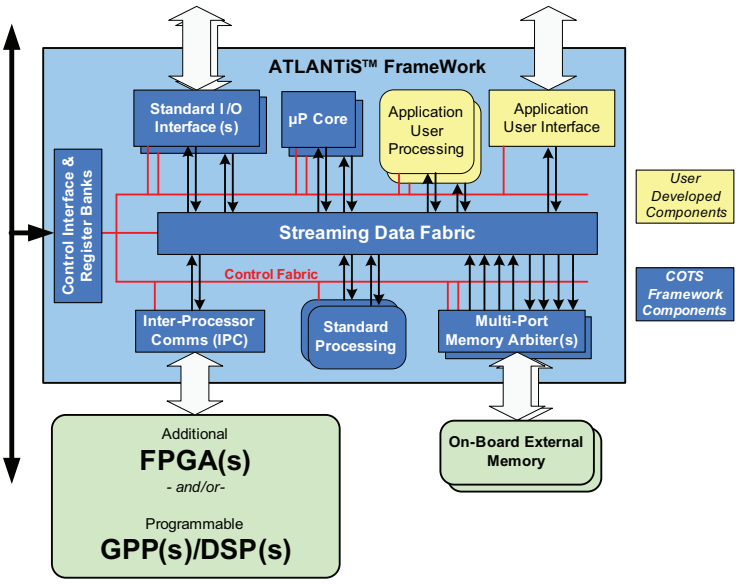
ATLANTiS FrameWork: Simplified FPGA Development

ATLANTiS FrameWork (AFW) is a library of FPGA components that includes preconfigured physical interfaces, infrastructure, and examples for BittWare's Altera FPGA-based COTS boards. In a typical FPGA design, physical interface development can account for the majority of the development time; however, AFW saves months of effort by providing critical physical interface components that are tested and configured to meet the BittWare board's specific requirements. To help further reduce development time, AFW includes many optional components for system IP, interconnect, and simulation and test. Working example projects for each supported board, which illustrate how to move data between the board's different interfaces, along with full simulation and synthesis example projects allow customers to have a board up and running within hours. AFW includes all source code and is provided with the BittWorks II Toolkit.

Development Tools

BittWare offers complete software support for the S5PH-Q with its BittWorks II software tools. BittWorks II is a suite of software development tools designed to make developing and debugging applications for BittWare's signal processing boards easy and efficient, regardless of whether the hardware is on the local machine or being accessed remotely. The BittWorks software tools include host interface libraries, a variety of diagnostic utilities and configuration tools, debug tools, and I/O drivers, all of which are tightly integrated with the ATLANTiS FrameWork.

Figure 1: ATLANTiS FrameWork Architecture Overview



S5PH-Q Specifications

Board Specifications

FPGA

- Altera® Stratix® V GX/GS FPGA
- Supported by BittWare's ATLANTiS™ FrameWork
- 20 full-duplex, high-performance, multi-gigabit SerDes transceivers @ up to 14.1 GHz
- Up to 952,000 logic elements (LEs) available
- Up to 62 Mb of embedded memory
- 1.4 Gbps LVDS performance
- Up to 3,926 18x18 variable-precision multipliers
- Embedded HardCopy Blocks

Anemone FPGA Co-processor

- One 16-core Anemone104 C-programmable floating point co-processor for FPGAs
- 750 MHz multicore processor
- 24 GFLOPS in 1 Watt core power

External Memory

- Two banks of up to 4 GByte DDR3 SDRAM (x64)
- Four banks of up to 18 MBytes QDRII+ (x18)
- 128 MBytes of Flash memory for booting FPGA

PCIe Interface

- x8 Gen1, Gen2, Gen3 direct to FPGA

USB Header

- USB 2.0 interface for debug and programming FPGA and Flash

Debug Utility Header

- RS-232 port to Stratix V
- JTAG debug interface to Stratix V

QSFP+ Cages

- 2 QSFP+ cages on front panel connected directly to FPGA via 8 SerDes (no external PHY)
- Each supports 40 GigE or four 10 GigE interfaces
- Can be optionally adapted for use as SFP+

Serial ATA

- 2 SATA connectors, connected to FPGA

Size

- Half-length, standard-height PCIe slot card

Development Tools

ATLANTiS FrameWork FPGA Development Kit

- Physical interface components
- Library of optional components for system, interconnect, simulation, and test IP
- Board, I/O, and timing constraints
- Example Quartus projects
- Full ModelSim simulations
- Software components and drivers

System Development

- BittWorks II Toolkit - host, command, and debug tools for BittWare hardware
- BittWorks II Porting Kit - source code and prebuilt ports for porting the BittWare Toolkit to other operating systems
- BWIO - software library for controlling I/O on BittWare boards

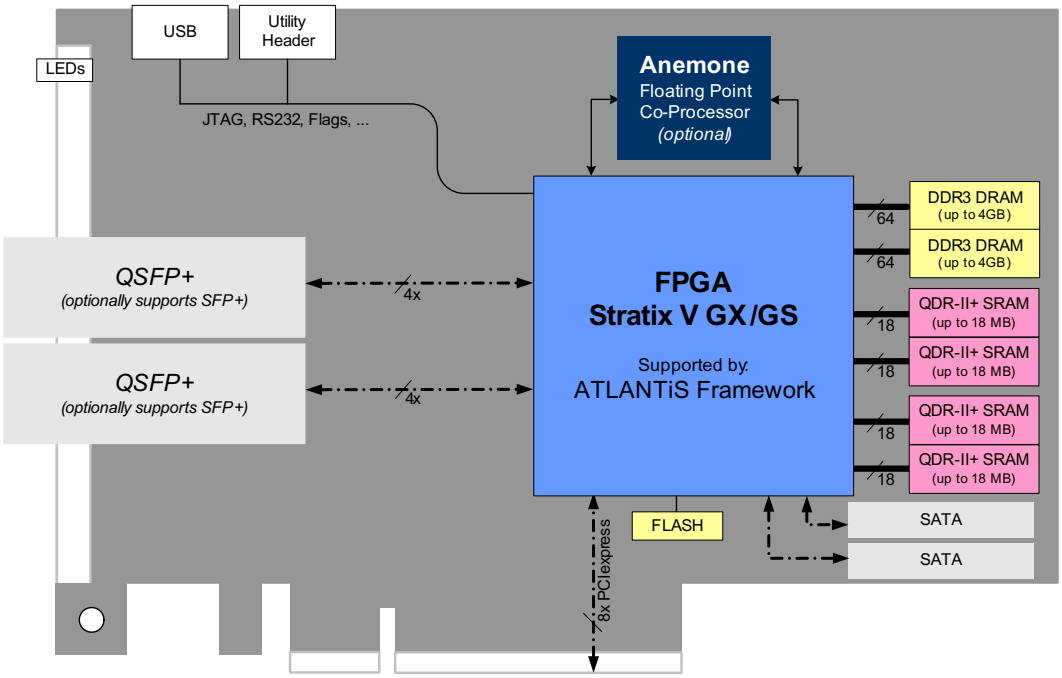
FPGA Development

- Altera Quartus® II software

Accessory Boards

- BittWare GXBO breakout board for JTAG and RS-232 access

Figure 2: S5PH-Q System Block Diagram



S5PH-Q Ordering Options

S5PHQ-RW-AAAAABCC-DEFHIJKLM-NOPQR

RW	Ruggedization 0U = Commercial (0C to 50C)* 2C = Conduction-cooled conformal coating (-40C to 75C)
AAAAA	S5 Family, Hardcopy, and Size 00000 = None GXEA3 = Stratix V GXEA3 GXEA4 = Stratix V GXEA4 GXEA5 = Stratix V GXEA5 GXEA7 = Stratix V GXEA7* GXEA9 = Stratix V GXEA9† GXEAB = Stratix V GXEAB† GSMD4 = Stratix V GSMD4 GSMD5 = Stratix V GSMD5 GSED6 = Stratix V GSED6† GSED8 = Stratix V GSED8†
B	S5 GXB Speed 0 = None 2 = 2 3 = 3*
CC	S5 Temp/Speed 00 = None C1= Commercial Temperature Range, Speed Grade 1 C2= Commercial Temperature Range, Speed Grade 2 C3= Commercial Temperature Range, Speed Grade 3* I3 = Industrial Temperature Range, Speed Grade 3 I4 = Industrial Temperature Range, Speed Grade 4*
D	DDR3 Bank A 0 = None 9 = 1GB A = 2 GB* B = 4 GB
E	DDR3 Bank B 0 = None 9 = 1GB A = 2 GB* B = 4 GB
F	QDR II Bank A 0 = None 2 = 9 MB* 3 = 18 MB
G	QDR II Bank A Type & Speed 0 = None 1 = QDR2 250MHz 2 = QDR2 300MHz* 3 = QDR2 333MHz A = QDR2+ 400MHz B = QDR2+ 450MHz C = QDR2+ 500MHz D = QDR2+ 550MHz
H	QDR II Bank B 0 = None 2 = 9 MB* 3 = 18 MB
I	QDR II Bank B Type & Speed 0 = None 1 = QDR2 250MHz 2 = QDR2 300MHz* 3 = QDR2 333MHz A = QDR2+ 400MHz B = QDR2+ 450MHz C = QDR2+ 500MHz D = QDR2+ 550MHz
J	QDR II Bank C 0 = None 2 = 9 MB* 3 = 18 MB
K	QDR II Bank C Type & Speed 0 = None 1 = QDR2 250MHz 2 = QDR2 300MHz* 3 = QDR2 333MHz A = QDR2+ 400MHz B = QDR2+ 450MHz C = QDR2+ 500MHz D = QDR2+ 550MHz
L	QDR II Bank D 0 = None 2 = 9 MB* 3 = 18 MB
M	QDR II Bank D Type & Speed 0 = None 1 = QDR2 250MHz 2 = QDR2 300MHz* 3 = QDR2 333MHz A = QDR2+ 400MHz B = QDR2+ 450MHz C = QDR2+ 500MHz D = QDR2+ 550MHz
N	Anemone 0 = None* 1 = AN104
O	Oscillator S = Standard* T = TCXO
P	Front Panel Options 0 = No SMA 1 = SMA CLKRef 2 = SMA FPGA
Q	Misc. Configuration 0 = Standard
R	Assembly F = Pb-free assembly* P = Pb assembly

*Default

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