XUPSVH

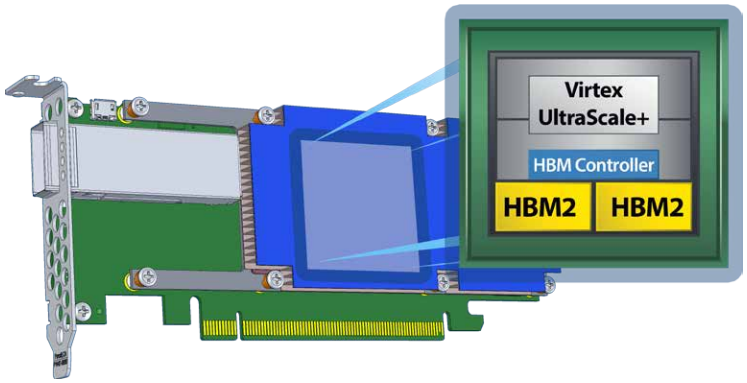
Xilinx UltraScale+ Low Profile PCIe Board

VU35P with Integrated HBM2 and 2x 100GbE on BittWare Spider Platform

Ultra high-speed network interface
2x 100GbE and timestamping support
Up to 4x 100GbE with standard-height option

Latest generation 16nm FPGA
UltraScale+ FPGA with integrated HBM2

Optimized for thermal performance
BittWare Spider platform with passive heatsink supports large FPGA loads



XILINX
ALLIANCE PROGRAM

BittWare's XUPSVH is an UltraScale+ VU33P/35P FPGA-based PCIe card ideal for high-density datacenter applications that demand high memory bandwidth. The UltraScale+ FPGA helps these demanding applications avoid I/O bottlenecks with integrated High Bandwidth Memory (HBM2) tiles on the FPGA that support up to 8 GBytes of memory at 460 GBytes/sec.

Along with the integrated memory, the UltraScale+ VU35P offers up to 1.9 million logic elements, which gives designers incredible performance potential — yet with a power density that makes thermal management difficult. The XUPSVH meets this challenge with BittWare's Spider platform, supporting large FPGA loads and 2x 100 Gbps Ethernet. Up to 4x 100 GbE is available with a standard-height option.

Spider Platform

The XUPSVH is designed with BittWare's Spider platform, which is a low-profile PCIe platform optimized for thermal performance. The Spider platform combines a low-profile PCIe form-factor for high density, the ability to run larger loads, and a robust passive heatsink option designed for servers.

Key Features

- Xilinx Virtex UltraScale+ VU33P/VU35P
- 8 GB Integrated High Bandwidth Memory (HBM2) @ 460 GBps
- PCIe x16 interface supporting Gen1, Gen2, or Gen3 or x8 Gen4
- Up to two QSFP-DD cages for 4x 40/100GbE or 16x 10/25GbE
- UltraPort SlimSAS™ for serial expansion
- Board Management Controller for Intelligent Platform Management
- FPGA examples and complete software support

High-Speed Networking and I/O

The XUPSVH is enabled for high-speed networking with up to two front panel QSFP Double Density (QSFP-DD) cages, each supporting two 40/100GbE or eight 10/25GbE channels. Serial expansion is available through an UltraPort SlimSAS connector (8x 24Gbps) that can be connected to a second PCIe interface, another XUPSVH, or other devices, including IBM's POWER9 via OpenCAPI. A utility header provides a 1GbE interface, a PPS input, and a USB interface for debug and programming support.

Board Management Controller

The XUPSVH features an advanced system monitoring subsystem, similar to those typically found on today's server platforms. At the heart of the board's monitoring system lies a Board Management Controller (BMC), which accepts Intelligent Platform Management Interface (IPMI) messaging protocol commands. The BMC provides a wealth of features, including control of power and resets, monitoring of board sensors, FPGA boot loader, voltage overrides, configuration of programmable clocks, access to I^2C bus components, field upgrades, and IPMI messaging. Access to the BMC is via PCIe or USB. BittWare's BittWorks II Toolkit also provides utilities and libraries for communicating with the BMC components at a higher, more abstract level, allowing developers to remotely monitor the health of the board.

Development Tools

BittWorks II Toolkit

BittWare offers complete software support for the XUPSVH with its BittWorks II software tools. The BittWorks II Toolkit is a suite of development tools that serves as the main interface between the BittWare board and the host system. The Toolkit includes drivers, libraries, utilities, and example projects for accessing, integrating, and developing applications for the BittWare board.

FPGA Example Projects

BittWare offers FPGA example projects to provide FPGA board support IP and integration for its UltraScale+ boards. The example projects easily integrate with the Xilinx Vivado tools and illustrate how to move data between the board's different interfaces. All examples are available for download on BittWare's developer website.

Specifications

Board Specifications

FPGA

- Virtex UltraScale+ VU33P/VU35P
- 40x GTY transceivers at 32.75 Gbps
- Up to 1.9 million logic elements
- 8 GBytes of HBM2 high-bandwidth DRAM
- Up to 5 integrated PCIe cores
- Up to 5,952 DSP slices with 27x18 multipliers

On-Board Memory

- Flash memory for booting FPGA

PCIe Interface

- x16 Gen1, Gen2, Gen3 interface direct to FPGA

Utility Header

- USB, 1 PPS input, 1GbE

UltraPort SlimSAS

- Standard high-speed connector for storage devices
- Connected to FPGA via 8x transceivers
- OpenCAPI compatible
- Can support an additional x8 PCIe interface (requires second slot)

QSFP-DD Cages

- 2 QSFP-DD cages (one is optional*) on front panel connected directly to FPGA via 16 transceivers
- Each supports 2x 40/100GbE and 8x 10/25GbE

Board Management Controller

- Voltage, current, temperature monitoring
- Power sequencing and reset
- Field upgrades
- FPGA configuration and control
- Clock configuration
- I^2C bus access
- USB 2.0 and JTAG access
- Voltage overrides

Size

- Low profile (Half-height*, half-length) PCIe slot card; x16 mechanical
- 168mm x 68.9mm
- Max. component height: 34.79mm dual slot

Development Tools

System Development

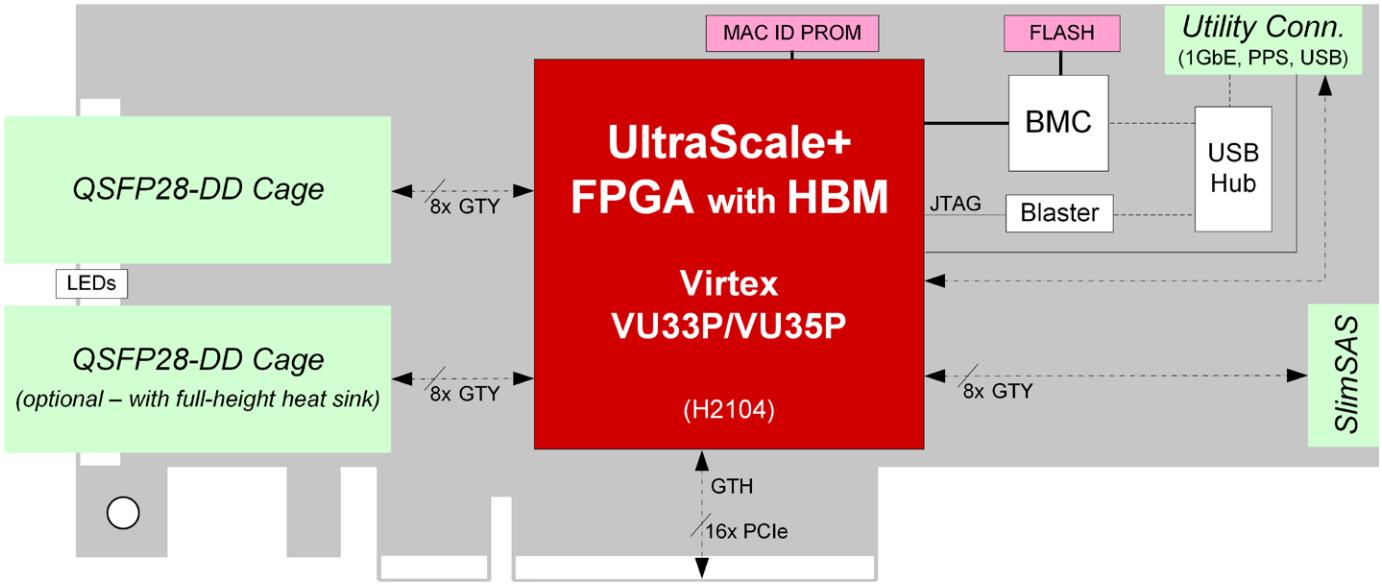
- BittWorks II Toolkit - host, command, and debug tools for BittWare hardware

FPGA Development

- FPGA DevKit - example Vivado projects
- Xilinx Tools - Vivado® Design Suite

* Second QSFP-DD option requires a standard-height heat sink.

Figure 2: XUPSVH System Block Diagram



XUPSVH Ordering Options

XUPSVH - [TBD*]

* Contact BittWare for availability

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