

# XUPVV4

## Xilinx UltraScale+ 3/4-Length PCIe Board VU13P with Quad QSFP and 512 GBytes DDR4 on BittWare Viper Platform

### Ultra high-speed network interface

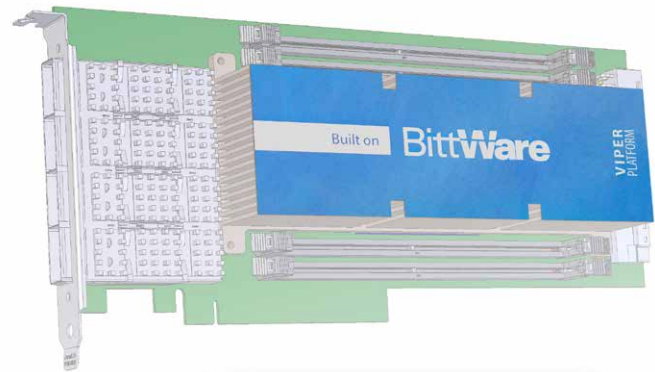
4x 100GbE and timestamping support

### Latest generation 16nm FPGA

UltraScale+ FPGA with up to 3.8 million LEs

### Optimized for thermal performance

BittWare Viper platform with passive heatsink supports large FPGA loads



BittWare's XUPVV4 is an UltraScale+ VU13P FPGA-based PCIe card, ideal for high-density datacenter applications. The Xilinx UltraScale+ VU13P FPGA gives designers incredible performance potential, with 3.8M logic elements —yet with a power density that makes thermal management difficult. The XUPVV4 meets this challenge with BittWare's Viper platform, supporting large FPGA loads, up to 512 GBytes DDR4, and 4x 100 Gbps Ethernet.

### Viper Platform and Lidless Package

BittWare's Viper platform uses advanced computer flow simulation to drive the physical board design in a thermals first approach, including the use of heat pipes, airflow channels, and arranging components to maximize the limited available airflow in a server. Viper boards are passive by default, with active cooling as an option. The XUPVV4 features the D2104 lidless package from Xilinx—allowing the heat pipes to contact the die directly, instead of through the heat spreader lid.

### Key Features

- Xilinx Virtex UltraScale+ VU13P
- PCIe x16 interface supporting Gen1, Gen2, or Gen3
- Four QSFP cages for 4x 40/100GbE or 16x 10/25GbE
- Up to 512 GBytes DDR4
- UltraPort SlimSAS™ for serial expansion
- Board Management Controller for Intelligent Platform Management
- FPGA examples and complete software support

## High-Speed Networking and I/O

The XUPVV4 is enabled for high-speed networking with four front panel QSFP+ cages, each supporting 40/100GbE or four 10/25GbE channels. Serial expansion is available through two UltraPort SlimSAS connectors (16x 24Gbps) that can be connected to a second PCIe interface, another XUPVV4, or other devices, including IBM's POWER9 via OpenCAPI. A utility header provides a 1GbE interface, a PPS input, and a USB interface for debug and programming support.

## Memory

The board's flexible memory configuration includes four DIMM sites that support DDR4 SDRAM and QDR. Memory card options include up to 128 GBytes of DDR4 with optional error-correcting codes (ECC) or up 576 Mbits QDR-II+ (2x 288Mbit banks x18). The board also features flash memory for FPGA images.

## Board Management Controller

The XUPVV4 features an advanced system monitoring subsystem, similar to those typically found on today's server platforms. At the heart of the board's monitoring system lies a Board Management Controller (BMC), which accepts Intelligent Platform Management Interface (IPMI) messaging protocol commands. The BMC provides a wealth of features, including control of power and resets, monitoring of board sensors, FPGA boot loader, voltage overrides, configuration of programmable clocks, access to I<sup>2</sup>C bus components, field upgrades, and IPMI messaging. Access to the BMC is via PCIe or USB. BittWare's BittWorks II Toolkit also provides utilities and libraries for communicating with the BMC components at a higher, more abstract level, allowing developers to remotely monitor the health of the board.

## Development Tools

### BittWorks II Toolkit

BittWare offers complete software support for the XUPVV4 with its BittWorks II software tools. The BittWorks II Toolkit is a suite of development tools that serves as the main interface between the BittWare board and the host system. The Toolkit includes drivers, libraries, utilities, and example projects for accessing, integrating, and developing applications for the BittWare board.

### FPGA Development Kit

BittWare's FPGA Development Kit (FDK) provides FPGA board support IP to simplify integration and development. The FDK includes example projects that illustrate how to move data between the board's different interfaces and is designed to integrate easily with the Xilinx Vivado tools. All examples are available for download on BittWare's developer website.

## Specifications

### BOARD SPECIFICATIONS

#### FPGA

- Virtex UltraScale+ VU13P
- 48x GTY transceivers at 32.75 Gbps
- Up to 3.8 million logic elements
- Over 400 Mb of embedded memory
- Up to 6 integrated PCIe cores
- Up to 11,904 DSP slices with 27x18 multipliers

#### On-Board Memory

- Flash memory for booting FPGA

#### Optional DIMM Memory

- 4 DIMM sites, each supporting:
  - Up to 128 GBytes DDR4 x72 with ECC
  - Up to 576 Mbits dual QDR-II+ x18 (2 independent 288 Mbit banks)

#### PCIe Interface

- x16 Gen1, Gen2, Gen3 interface direct to FPGA

#### Utility Header

- USB, 1 PPS input, 1GbE

#### UltraPort SlimSAS

- Standard high-speed connector for storage devices
- Connected to FPGA via 8x transceivers
- OpenCAPI compatible
- Can support an additional x16 or x8 PCIe interface (requires second slot)

#### QSFP Cages

- 4 QSFP28 (zQSFP) cages on front panel connected directly to FPGA via 16 transceivers
- Each supports 100GbE, 40GbE, 4x 25GbE, or 4x 10GbE and can be combined for 400GbE

#### Board Management Controller

- Voltage, current, temperature monitoring
- Power sequencing and reset
- Field upgrades
- FPGA configuration and control
- Clock configuration
- I<sup>2</sup>C bus access
- USB 2.0 and JTAG access
- Voltage overrides

#### Size

- 3/4-length, standard-height PCIe dual-slot card
- 241mm x 111.15mm
- Max. component height: 34.79mm dual slot

#### DEVELOPMENT TOOLS

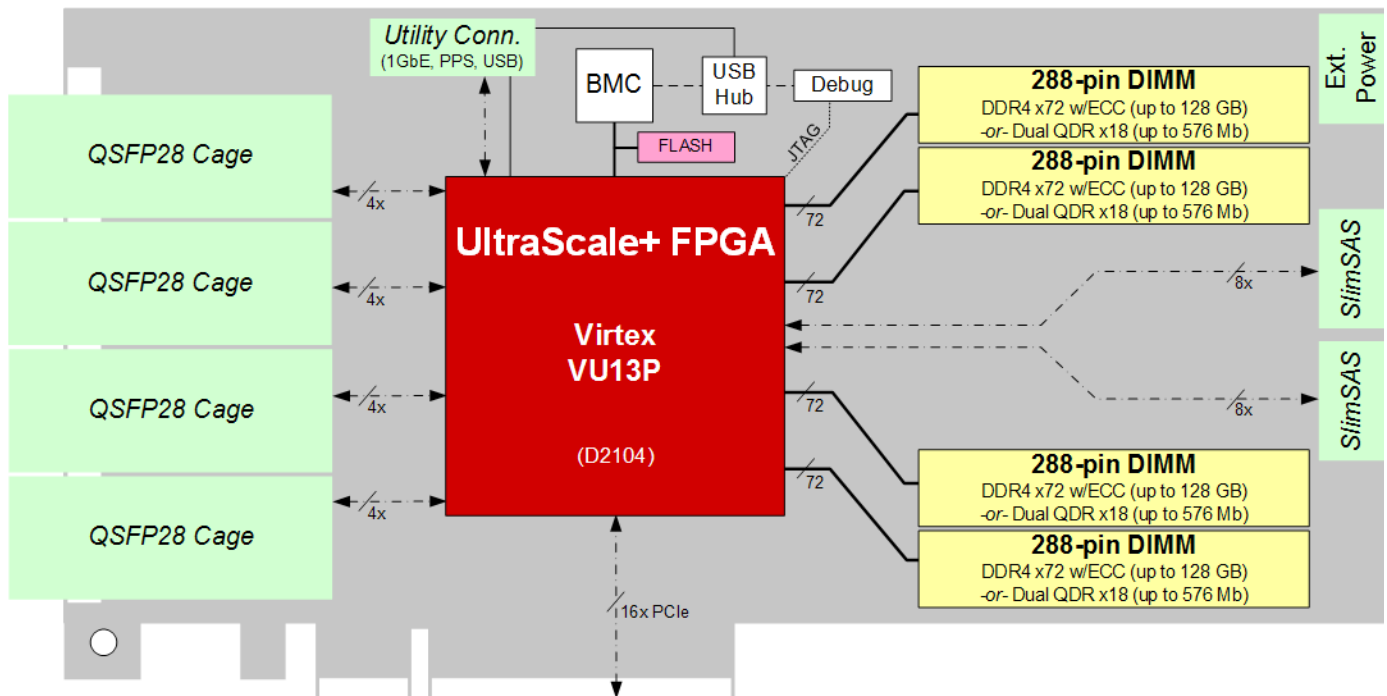
##### System Development

- [BittWorks II Toolkit](#) - host, command, and debug tools for BittWare hardware

##### FPGA Development

- [FPGA DevKit](#) - example Vivado projects
- [Xilinx Tools](#) - Vivado® Design Suite

Figure 2: XUPVV4 System Block Diagram



# XUPVV4

## XUPVV4 Ordering Options

XUPVV4 - [TBD\*]

\* Contact BittWare for availability

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